## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No	
Priority Filing Date	
Inventor	•
Assignee	Micron Technology, Inc.
Priority Group Art Unit	
Priority Examiner	
Attorney's Docket No	
Title: Gated Semiconductor Assemblies Semiconductor Assemblies	and Methods of Forming Gated

## INFORMATION DISCLOSURE STATEMENT PURSUANT TO 37 C.F.R. §§ 1.56, 1.97 AND 1.98

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a continuation application of co-pending application Serial No. 09/438,310, filed November 10, 1999. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. § 1.98(d) and MPEP § 609(2).

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: 30 Jan 2004

By:

Reg. No. 44,854

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY, DOCKET NO. MI22-2478			Priority SERIAL NO. 09/438,310				
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	AB	5,04:	5,847	9/91	Tarui et al.						
	AC	5,045	5,345	9/91	Singer	Singer					
	AD	4,996	6,081	2/91	Ellul et al.						
	AE	3,884	1,698	5/75	Kakihama et al.	Kakihama et al.					
	AF	5,518	8,946	5/96	Kuroda						
	AG	5,489	9,542	2/96	Iwai et al.						
	AH	4,330	0,569	5/82	Gulett et al.						
	Al	4,499	9,656	2/85	Fabian et al.						
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	AK	5,92	6,739	7/99	Rolfson et al.						
	AL	4,874	4,716	10/89	Rao			<b></b>	$\exists$		
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	AR		Silicon Proc. for VLS	SI; 177-178; Vol.	1; S. Wolf						
	AS		Silicon Proc. for VLS	SI; 191-193; Vol.	l; S. Wolf						
	AT		Silicon Proc. for VLS	SI; 37-38; 598-599	r, Vol. 2; S. Wolf						
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	АВ	4,439,270	3/84	Powell et al.						
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	AQ	Electronic Materials	Science: For Integ	rated Circuits; 1990 ©; Mayer et al;	pp. 269-274; Pub. I990					
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	AR	Intrinsic Stress in Si MA; June 5-8, 1988;	icon Nitride and :	Silicon Dioxide Films Prepared by \ J. et al.	arious Deposition Techn	iques; 1988	IEEE Internati.	Sympos. On	Electrical Insulation	
	AS	Passivation of GaAss 1418	FET's with PECV	D Silicon Nitride Films of Different	Stress States; IEEE Tran	sactions on	Electron Device	es; Vol. 35, N	o. 9; Sept. 1983; p	
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If Appropriate Date \*Examiner Document Name Class Subclass Initial Number 12/84 4,485,553 Christian et al. AA ΑB 4,543,707 10/85 Ito et al. 5,098,865 Machado et al AC 3/92 ΑD 5,160,998 11/92 Itoh et al. ΑE 5,306,946 4/94 Yamamoto ΑF 5,442,223 8/95 Fujii AG 5,523,616 6/96 Den ΑH 5,756,404 5/98 Friedenreich et. ΑI 5,834,374 11/98 Cabral Jr. et al ΑJ 4,695,872 9/87 Chatterjee AK 5,178,016 1/93 Dauenhauer et. AL 5,985,771 11/99 Moore et al. FOREIGN PATENT DOCUMENTS Document Date Subclass Country Translation Number Yes No AM ΑN ΑO ΑP AQ OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.) AR Silicon Nitride Overcoats for Thin Film Magnetic Recording Media; IEEE Transactions on Magnetics; Vol 27. No. 6, Nov. 1991; pp. 5070-5072 AS

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	AE	5,041,888	08/91	Possin et al.				_			
	AF	6,143,662	11/00	Rhodes et al.							
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